EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jose M. Nunez on March 25, 2009.

The application has been amended as follows:

IN THE CLAIMS:

Please see attached.

2. The following is an examiner's statement of reasons for allowance: The prior art does not teach nor render obvious each and every limitation of the claimed invention. Specifically the prior art fails to teach a pipeline of processors processing a data packet to remove layers of a data packet wherein each of the plurality of distinct processors include alignment circuitry to align a lowest significant bit of an operand, the alignment circuitry extending the operand to a defined bit width for processing by an arithmetic logic unit in the each of the plurality of processors.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHILIP J. CHEA whose telephone number is (571)272-3951. The examiner can normally be reached on M-F 6:30-4:00 (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on 571-272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Philip J Chea
Examiner
Art Unit 2453

/Philip J Chea/
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3/26/09

/ARIO ETIENNE/
Supervisory Patent Examiner, Art Unit 2457

1. (Currently Amended) A method for efficiently processing layers of a data packet, comprising:

defining a pipeline of processors in communication with a distributed network and a central processing unit (CPU) of a host system, the pipeline of processors consisting of multiple separate processors;

receiving a data packet from the distributed network into a first stage of one of the multiple separate processors of the pipeline of processors;

processing the data packet to remove a header associated with the first stage, the processing the data packet including aligning a lowest significant bit of an operand to a defined bit width for processing by an arithmetic logic unit in the processor from the multiple separate processors processing the data packet;

transmitting the processed data packet to a second stage associated with another one of the multiple separate processors for processing associated with the second stage;

repeating the operations of processing the data packet and transmitting the processed data packet for successive stages associated with corresponding processors until a header associated with a final stage has been removed from the data packet; and

transmitting the data packet from the final stage to the CPU of the host system.

2. (Original) The method of claim 1, wherein the data packet is an Ethernet data packet.

3. (Previously Presented) The method of claim 1, wherein each processor of the pipeline of processors includes at least three separate buffers configured to maintain a line rate, the three separate buffers receiving input from a common multiplexer.

4. (Original) The method of claim 1, wherein the successive stages correspond to layers of the data packet.

5. (Original) The method of claim 4, wherein the layers are selected from the group consisting of an IP layer, an IP SEC layer, a TCP layer, and an ISCSI layer.

6. (Original) The method of claim 1, wherein the method operation of processing the data packet to remove a header associated with the first stage includes,

defining instructions for processing the data packet; and

enabling an arithmetic logic unit (ALU) associated with each processor to process the instructions.

7. (Original) The method of claim 6, wherein the method operation of enabling an arithmetic logic unit (ALU) associated with each processor to process the instructions includes,

aligning the instructions by a least significant bit; and

extending each of the instructions to a defined bit size.

8. (Currently Amended) An adapter card configured to be in communication with a general purpose computer, comprising:

a plurality of distinct processors arranged in a pipeline architecture, the plurality of distinct processors defining a receiving pipeline and a transmitting pipeline, each processor of the plurality of distinct processors associated with a pipeline stage, each pipeline stage configured to process a layer of a data packet, wherein the receiving pipeline removes layers from the data packet and the transmitting pipeline adds layers to the data packet, wherein each of the plurality of distinct processors include alignment circuitry configured to align a lowest significant bit of an operand, the alignment circuitry extending the operand to a defined bit width for processing by an arithmetic logic unit in the each of the plurality of distinct processors.

9. (Original) The adapter card of claim 8, wherein the pipeline stage is associated with a layer of an Ethernet packet header.

10. (Original) The adapter card of claim 9, wherein the layer is selected from the group consisting of an IP layer, an IP SEC layer, a TCP layer, and an ISCSI layer.

11. (Original) The adapter card of claim 8, wherein the adapter card is a network interface card.

12. (Previously Presented) The adapter card of claim 8, wherein each of the plurality of processors include at least three separate buffers for maintaining an incoming line rate, the three separate buffers receiving input from a common multiplexer.

13. (Original) The adapter card of claim 8, wherein each of the plurality of processors include alignment circuitry configured to align a lowest significant bit of an operand, the alignment circuitry extending the operand to a defined bit width so that a pre-extending bit width of the operand is transparent to an arithmetic logic unit configured to process the operand.

14. (Currently Amended) A general purpose computer, comprising:

a central processing unit (CPU);

a network interface card (NIC) configured to process data packets, the NIC including,

a plurality of distinct processors arranged in a pipeline architecture, the plurality of distinct processors defining a receiving pipeline and a transmitting pipeline, each processor of the plurality of distinct processors associated with a pipeline stage, each pipeline stage configured to process a header associated the data packets, wherein each of the distinct processors of the receiving pipeline removes

headers from the data packets and each of the distinct processors of the transmitting pipeline adds headers to the data packets, wherein each of the plurality of processors include alignment circuitry configured to align a lowest significant bit of an operand, the alignment circuitry extending the operand to a defined bit width for processing by an arithmetic logic unit in the each of the plurality of processors.

15. (Original) The general purpose computer of claim 14, wherein the pipeline stage is associated with a layer of a header of the data packets.

16. (Original) The general purpose computer of claim 15, wherein the layer of the header of the data packets is selected from the group consisting of an IP layer, an IP SEC layer, a TCP layer, and an ISCSI layer.

17. (Previously Presented) The general purpose computer of claim 14, wherein each of the plurality of processors have at least three separate buffers configured to maintain an incoming line rate, the three separate buffers receiving input from a common multiplexer.

18. (Cancelled)

19. (Original) The general purpose computer of claim 14, wherein each of the plurality of processors are configured to execute a two stage pipeline process.

20. (Original) The general purpose computer of claim 14, wherein each of the data packets have a variable packet size.